

DDR SDRAM DIMM

D35PA56A2 – 256MB

For the latest data sheet, please visit the Super Talent Electronics web site: www.supertalentmemory.com

Features:

- 6 layer PCB
- 433MHz Double Data Rate = 3,500 Mb/sec
- CAS Latency (CL) 2.0
- RAS to CAS Delay (tRCD) 3
- Precharge Delay (tRP) 3
- 2.5volts - 2.8volts
- Double-data-rate architecture; 2 data transfers per clock cycle
- Serial Presence Detect with EEPROM
- Edge aligned data output, center aligned input
- Lifetime warranty
- Heat Spreader

Ratings:

Ambient Temperature (TA): 0 ~ 70 °C
 Storage Temperature (TSTG): -55 ~ 125 °C
 Voltage on Any Pin relative to VSS VIN,
 VOUT: -0.5 ~ 3.6 V
 Voltage on VDD relative to VSS VDD: -0.5 ~ 3.6 V
 Voltage on VDDQ relative to VSS VDDQ: -0.5 ~ 3.6 V
 Output Short Circuit Current (IOS): 50 mA
 Power Dissipation (PD): 9.5 W

Description:

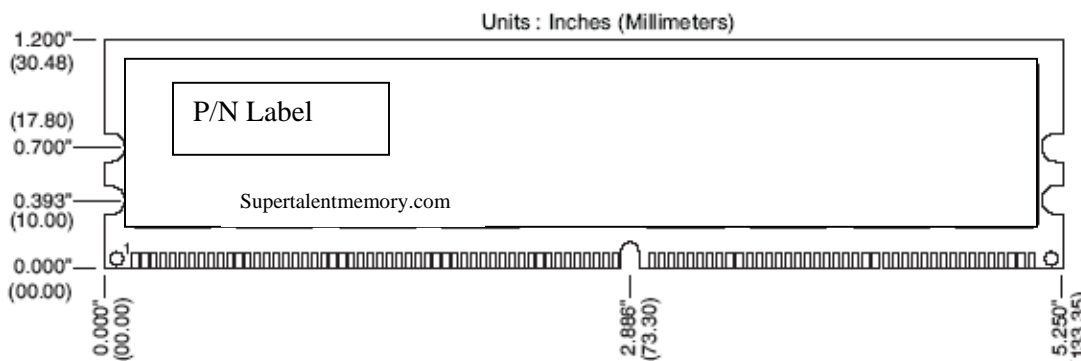
SuperTalent's D35PA56A2 is a 256MB, PC3500, 32M bit x 64, Double Data Rate SDRAM memory module. The module is built with eight 32M x 8 bit 66pin TSOP-II (400 mil) Double Data Rate SDRAM chips in a single bank, single sided configuration mounted on a 6-layer 184pin glass-epoxy substrate PCB.

The RAM has been tested in-house on the following chipsets: VIA K8T800, Intel 875P, ATI RS300 and NVidia NForce3 150 chipsets.

Characteristics:

Row Cycle Time (tRC): 55ns
 Auto Refresh Row Cycle Time (tRFC): 70ns
 Row Active Time (tRAS): 40ns min 70K ns max
 Row Address to Column Address Delay (tRCD): 15ns
 Row Active to Row Active Delay (tRRD): 10ns
 Column Address to Column Address Delay (tCCD): 1 CLK
 Row Precharge Time (tRP): 15 ns
 Write Recovery Time (tWR): 15 ns
 Last Data-In to Read Command (tDRL): 1 CLK
 Auto Precharge Write Recovery + Precharge Time (tDAL): 30 ns
 System Clock Cycle Time (tCK):
 CAS Latency = 3: 5ns min 10ns max
 CAS Latency = 2.5: 6ns min 10ns max
 CAS Latency = 2: 7.5ns min 10ns max
 Clock High Level Width (tCH): 0.45CLK min 0.55CLK max
 Clock Low Level Width (tCL): 0.45CLK min 0.55CLK max
 Data-Out edge to Clock edge Skew (tAC): -0.7ns min 0.7ns max
 DQS-Out edge to Clock edge Skew (tDQSCK): -0.60ns min 0.60ns max
 DQS-Out edge to Data-Out edge Skew (tDQSQ): 0.4ns max

Module Dimensions:



Module comes with heat spreader installed