

# DDR3 Registered/ECC DIMM Module

**1GB based on 1Gbit component**

**82FBGA with Pb-Free**



**Revision 1.0 (May, 2008)**  
-Initial Release

**1.0 Feature**

- JEDEC standard  $V_{DDQ}=1.5V \pm 0.075V$  Power Supply
- $V_{DDQ} = 1.5V \pm 0.075V$
- Programmable CAS Latency: 6,7,8,9,10,11
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 5(DDR3-800), 6(DDR3-1066), 7(DDR3-1333) and 8(DDR3-1600)
- 400MHz fCK for 800Mb/sec/pin, 533MHz fCK for 1066Mb/sec/pin, 667MHz fCK for 1333Mb/sec/pin, 800MHz fCK for 1600Mb/sec/pin
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm  $\pm$  1%)
- Bi-directional Differential Data Strobe
- Asynchronous Reset
- On-Die termination using ODT pin
- 8 independent internal bank
- Average Refresh Period 7.8us at lower than a TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
- Serial presence detect with EEPROM
- RDIMM Dimension (Nominal) 30.00 mm high, 133.35 mm wide
- Based on JEDEC standard reference Raw Cards Lay out.
- RoHS compliant
- Gold plated contacts

**2.0 Ordering Information**

| Part number | Density | Module Organization | Component composition | Component PKG | Module Rank | Description |
|-------------|---------|---------------------|-----------------------|---------------|-------------|-------------|
| W13RA1G8x   | 1GB     | 128Mx72             | 128Mx8*9              | FBGA          | 1           | PC3-10600   |

Note: Last Character x of the Part Number stand for DRAM vendor  
S=Samsung; M=Micron; H=Hynix

**3.0 Operating Frequencies**

|             | DD3-1333 | Unit |
|-------------|----------|------|
| CL-tRCD-tRP | 9-9-9    | tCK  |
| CAS Latency | 9        | tCK  |
| tCK(min)    | 1.5      | ns   |
| tRCD(min)   | 13.5     | ns   |
| tRP(min)    | 13.5     | ns   |
| tRAS(min)   | 36       | ns   |
| tRC(min)    | 49.5     | ns   |

**4.0 Absolute Maximum DC Rating**

| Symbol            | Parameter   | Rating       | Units |
|-------------------|---|--------------|-------|
| $V_{in}, V_{out}$ | Voltage on any pin relative to $V_{SS}$                     | -0.4 ~ 1.975 | V     |
| $V_{DD}$          | Voltage on $V_{DD}$ & $V_{DDQ}$ supply relative to $V_{SS}$ | -0.4 ~ 1.975 | V     |
| $V_{DDQ}$         | Short circuit current                                       | -0.4 ~ 1.975 | V     |
| $V_{DDL}$         | Power dissipation   | -0.4 ~ 1.975 | V     |
| $T_{STG}$         | Storage Temperature   | -55 ~ + 100  | °C    |

**5.0 DIMM Pin Configurations (Front side/Back side)**

| Pin | Front                    | Pin | Back                      | Pin | Front                        | Pin | Back                      | Pin | Front                    | Pin | Back                      | Pin  | Front                    | Pin | Back                      |
|-----|--------------------------|-----|---------------------------|-----|------------------------------|-----|---------------------------|-----|--------------------------|-----|---------------------------|------|--------------------------|-----|---------------------------|
| 1   | V <sub>REFDQ</sub>       | 121 | V <sub>SS</sub>           | 31  | DQ25                         | 151 | V <sub>SS</sub>           | 61  | A2                       | 181 | A1                        | 91   | DQ41                     | 211 | V <sub>SS</sub>           |
| 2   | V <sub>SS</sub>          | 122 | DQ4                       | 32  | V <sub>SS</sub>              | 152 | DQS12                     | 62  | V <sub>DD</sub>          | 182 | V <sub>DD</sub>           | 92   | V <sub>SS</sub>          | 212 | DQS14                     |
| 3   | DQ0                      | 123 | DQ5                       | 33  | $\overline{\text{DQS3}}$     | 153 | $\overline{\text{DQS12}}$ | 63  | NC                       | 183 | V <sub>DD</sub>           | 93   | $\overline{\text{DQS5}}$ | 213 | $\overline{\text{DQS14}}$ |
| 4   | DQ1                      | 124 | V <sub>SS</sub>           | 34  | DQS3                         | 154 | V <sub>SS</sub>           | 64  | NC                       | 184 | CK0                       | 94   | DQS5                     | 214 | V <sub>SS</sub>           |
| 5   | V <sub>SS</sub>          | 125 | DQS9                      | 35  | V <sub>SS</sub>              | 155 | DQ30                      | KEY |                          |     |                           | 95   | V <sub>SS</sub>          | 215 | DQ46                      |
| 6   | $\overline{\text{DQS0}}$ | 126 | $\overline{\text{DQS9}}$  | 36  | DQ26                         | 156 | DQ31                      | 65  | V <sub>DD</sub>          | 185 | $\overline{\text{CK0}}$   | DQ47 | DQ42                     | 216 | DQ47                      |
| 7   | DQS0                     | 127 | V <sub>SS</sub>           | 37  | DQ27                         | 157 | V <sub>SS</sub>           | 66  | V <sub>DD</sub>          | 186 | V <sub>DD</sub>           | 97   | DQ43                     | 217 | V <sub>SS</sub>           |
| 8   | V <sub>SS</sub>          | 128 | DQ6                       | 38  | V <sub>SS</sub>              | 158 | CB4                       | 67  | V <sub>REFCA</sub>       | 187 | $\overline{\text{EVENT}}$ | 98   | V <sub>SS</sub>          | 218 | DQ52                      |
| 9   | DQ2                      | 129 | DQ7                       | 39  | CB0                          | 159 | CB5                       | 68  | NC/Par_in                | 188 | A0                        | 99   | DQ48                     | 219 | DQ53                      |
| 10  | DQ3                      | 130 | V <sub>SS</sub>           | 40  | CB1                          | 160 | V <sub>SS</sub>           | 69  | V <sub>DD</sub>          | 189 | V <sub>DD</sub>           | 100  | DQ49                     | 220 | V <sub>SS</sub>           |
| 11  | V <sub>SS</sub>          | 131 | DQ12                      | 41  | V <sub>SS</sub>              | 161 | DQS17                     | 70  | A10/AP                   | 190 | BA1                       | 101  | V <sub>SS</sub>          | 221 | DQS15                     |
| 12  | DQ8                      | 132 | DQ13                      | 42  | $\overline{\text{DQS8}}$     | 162 | $\overline{\text{DQS17}}$ | 71  | BA0                      | 191 | V <sub>DD</sub>           | 102  | $\overline{\text{DQS6}}$ | 222 | $\overline{\text{DQS15}}$ |
| 13  | DQ9                      | 133 | V <sub>SS</sub>           | 43  | DQS8                         | 163 | V <sub>SS</sub>           | 72  | V <sub>DD</sub>          | 192 | $\overline{\text{RAS}}$   | 103  | DQS6                     | 223 | V <sub>SS</sub>           |
| 14  | V <sub>SS</sub>          | 134 | DQS10                     | 44  | V <sub>SS</sub>              | 164 | CB6                       | 73  | $\overline{\text{WE}}$   | 193 | $\overline{\text{S0}}$    | 104  | V <sub>SS</sub>          | 224 | DQ54                      |
| 15  | $\overline{\text{DQS1}}$ | 135 | $\overline{\text{DQS10}}$ | 45  | CB2                          | 165 | CB7                       | 74  | $\overline{\text{CAS}}$  | 194 | V <sub>DD</sub>           | 105  | DQ50                     | 225 | DQ55                      |
| 16  | DQS1                     | 136 | V <sub>SS</sub>           | 46  | CB3                          | 166 | V <sub>SS</sub>           | 75  | V <sub>DD</sub>          | 195 | ODT0                      | 106  | DQ51                     | 226 | V <sub>SS</sub>           |
| 17  | V <sub>SS</sub>          | 137 | DQ14                      | 47  | V <sub>SS</sub>              | 167 | NC                        | 76  | NC                       | 196 | A13                       | 107  | V <sub>SS</sub>          | 227 | DQ60                      |
| 18  | DQ10                     | 138 | DQ15                      | 48  | V <sub>TT</sub>              | 168 | $\overline{\text{RESET}}$ | 77  | NC                       | 197 | V <sub>DD</sub>           | 108  | DQ56                     | 228 | DQ61                      |
| 19  | DQ11                     | 139 | V <sub>SS</sub>           | 49  | V <sub>TT</sub>              | 169 | NC                        | 78  | V <sub>DD</sub>          | 198 | NC                        | 109  | DQ57                     | 229 | V <sub>SS</sub>           |
| 20  | V <sub>SS</sub>          | 140 | DQ20                      | 50  | CKE0                         | 170 | V <sub>DD</sub>           | 79  | NC                       | 199 | V <sub>SS</sub>           | 110  | V <sub>SS</sub>          | 230 | DQS16                     |
| 21  | DQ16                     | 141 | DQ21                      | 51  | V <sub>DD</sub>              | 171 | A15                       | 80  | V <sub>SS</sub>          | 200 | DQ36                      | 111  | $\overline{\text{DQS7}}$ | 231 | $\overline{\text{DQS16}}$ |
| 22  | DQ17                     | 142 | V <sub>SS</sub>           | 52  | BA2                          | 172 | A14                       | 81  | DQ32                     | 201 | DQ37                      | 112  | DQS7                     | 232 | V <sub>SS</sub>           |
| 23  | V <sub>SS</sub>          | 143 | DQS11                     | 53  | $\overline{\text{ERR\_OUT}}$ | 173 | V <sub>DD</sub>           | 82  | DQ33                     | 202 | V <sub>SS</sub>           | 113  | V <sub>SS</sub>          | 233 | DQ62                      |
| 24  | $\overline{\text{DQS2}}$ | 144 | $\overline{\text{DQS11}}$ | 54  | V <sub>DD</sub>              | 174 | A12                       | 83  | V <sub>SS</sub>          | 203 | DQS13                     | 114  | DQ58                     | 234 | DQ63                      |
| 25  | DQS2                     | 145 | V <sub>SS</sub>           | 55  | A11                          | 175 | A9                        | 84  | $\overline{\text{DQS4}}$ | 204 | DQS13                     | 115  | DQ59                     | 235 | VSS                       |
| 26  | V <sub>SS</sub>          | 146 | DQ22                      | 56  | A7                           | 176 | V <sub>DD</sub>           | 85  | DQS4                     | 205 | V <sub>SS</sub>           | 116  | V <sub>SS</sub>          | 236 | V <sub>DD</sub> SPD       |
| 27  | DQ18                     | 147 | DQ23                      | 57  | V <sub>DD</sub>              | 177 | A8                        | 86  | V <sub>SS</sub>          | 206 | DQ38                      | 117  | SA0                      | 237 | SA1                       |
| 28  | DQ19                     | 148 | V <sub>SS</sub>           | 58  | A5                           | 178 | A6                        | 87  | DQ34                     | 207 | DQ39                      | 118  | SCL                      | 238 | SDA                       |
| 29  | V <sub>SS</sub>          | 149 | DQ28                      | 59  | A4                           | 179 | V <sub>DD</sub>           | 88  | DQ35                     | 208 | V <sub>SS</sub>           | 119  | SA2                      | 239 | V <sub>SS</sub>           |
| 30  | DQ24                     | 150 | DQ29                      | 60  | V <sub>DD</sub>              | 180 | A3                        | 89  | V <sub>SS</sub>          | 209 | DQ44                      | 120  | V <sub>TT</sub>          | 240 | V <sub>TT</sub>           |
|     |                          |     |                           |     |                              |     |                           | 90  | DQ40                     | 210 | DQ45                      |      |                          |     |                           |

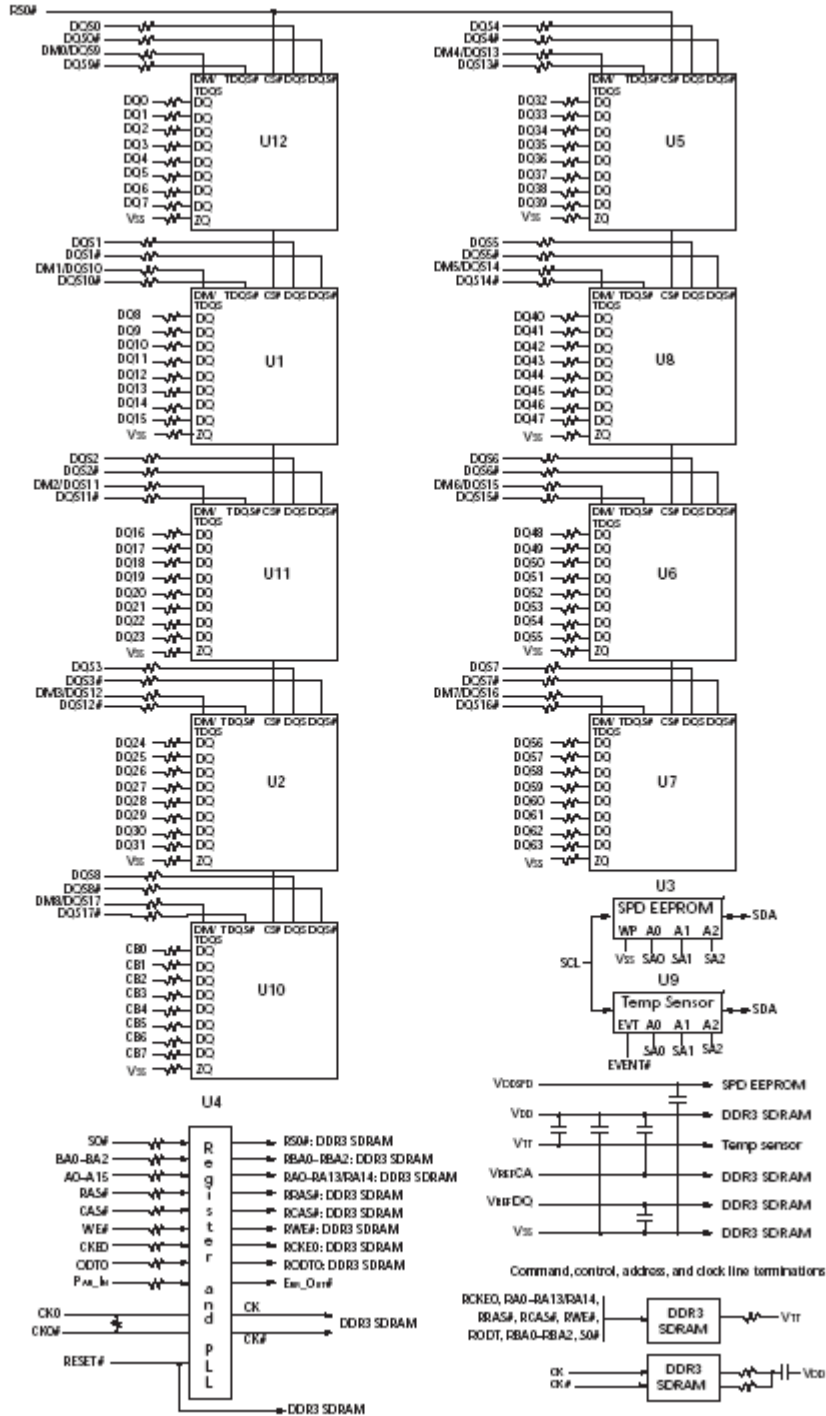
**6.0 DIMM Pin Description**

| Pin Name  | Function                                    | Pin Name                               | Function                            |
|---|---|--|-------------------------------------|
| A0 ~ A15  | Address input (Multiplexed)                 | ODT0~ODT1                              | On Die Termination                  |
| A10/AP  | Address Input/Auto pre-charge               | CB0~CB7                                | ECC Data check bits Input/Output    |
| BA0 ~ BA2   | Bank Select                                 | DQ0~DQ63                               | Data Input/Output                   |
| $\overline{CK0} \sim \overline{CK2}$ ,<br>CK0~CK2 | Clock input                                 | $\overline{DQS0} \sim \overline{DQS8}$ | Data strobes, negative line         |
| CKE0, CKE1  | Clock enable input                          | DM (0~8),                              | Data Masks/Data strobes (Read)      |
| $\overline{S0}$ , $\overline{S1}$                 | Chip select input                           | DQS0~DQS8                              | Data Strobes                        |
| $\overline{RAS}$                                  | Row address strobe                          | RFU                                    | Reserved for future used            |
| $\overline{CAS}$                                  | Column address strobe                       | V <sub>TT</sub>                        | SDRAM I/O termination power supply  |
| $\overline{WE}$                                   | Write Enable                                | TEST                                   | Memory bus test tool                |
| SCL   | SPD Clock Input                             | V <sub>DD</sub>                        | Core Power                          |
| SDA   | SPD Data Input/Output                       | V <sub>DDQ</sub>                       | I/O Power                           |
| SA0~SA2   | SPD Address                                 | V <sub>SS</sub>                        | Ground                              |
| Par_In  | Parity bit for address & Control bus        | V <sub>REFDQ</sub>                     | SDRAM Input/Output Reference Supply |
| $\overline{EVENT}$                                | EVENT pin on TS/SPD part, Temperature event | V <sub>DDSPD</sub>                     | Serial EEPROM Power Supply          |
| Reset   | Register and PLL control pin                | V <sub>REFCA</sub>                     | Command Address Reference Supply    |

**7.0 Address Configuration**

| Organization    | Row Address | Column Address | Bank Address | Auto Pre-charge |
|-----------------|-------------|----------------|--------------|-----------------|
| 128Mx8(1Gb)base | A0-A13      | A0-A9          | BA0-BA2      | A10             |

**8.0 Functional Block Diagram: 1GB; 128x72 Module (Populated as 1 rank of x8 SDRAM Module)**



Note: 1. The ZQ ball on each DDR3 component is connected to an external  $240\Omega \pm 1\%$  resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

**9.0 AC & DC Operating Conditions**

Recommended operating conditions (Voltage referenced to V<sub>SS</sub>=0V, TA=0 to 70°C)

| Symbol                 | Parameter                       | Min                   | Typ                   | Max                   | Unit |
|------------------------|---------------------------------|-----------------------|-----------------------|-----------------------|------|
| V <sub>DD</sub>        | Supply Voltage                  | 1.425                 | 1.5                   | 1.575                 | V    |
| V <sub>DDQ</sub>       | Supply Voltage for Output       | 1.425                 | 1.5                   | 1.575                 | V    |
| V <sub>REFDQ(DC)</sub> | I/O Reference Voltage (DQ)      | 0.49*V <sub>DDQ</sub> | 0.50*V <sub>DDQ</sub> | 0.51*V <sub>DDQ</sub> | V    |
| V <sub>REFCA(DC)</sub> | I/O Reference Voltage (CMD/Add) | 0.49*V <sub>DDQ</sub> | 0.50*V <sub>DDQ</sub> | 0.51*V <sub>DDQ</sub> | V    |
| V <sub>TT</sub>        | Termination Voltage             | 0.49*V <sub>DDQ</sub> | 0.50*V <sub>DDQ</sub> | 0.51*V <sub>DDQ</sub> | V    |

**10.0 Capacitance (Max.)**

| Symbol | Parameter/Condition                                     | Min | Max | Unit |
|--------|---|-----|-----|------|
| CCK    | Input capacitance, CK and $\overline{\text{CK}}$        | -   | 11  | pF   |
| CI1    | Input capacitance, CKE and $\overline{\text{CS}}$       | -   | 12  | pF   |
| CI2    | Input capacitance, Addr, RAS, CAS, WE                   | -   | 12  | pF   |
| CIO    | Input capacitance, DQ, DM, DQS, $\overline{\text{DQS}}$ | -   | 10  | pF   |

**11.1 AC Timing Parameters & Specifications**

(AC operating conditions unless otherwise noted)

| Parameter  | Symbol                     | DDR3-1333   |   | Units                |
|--|----------------------------|---|---|----------------------|
|  |                            | min   | max   |                      |
| Minimum Clock Cycle Time (DLL off mode)                | t <sub>CK(DLL_OFF)</sub>   | 8   | -   | ns                   |
| Average Clock Period                                   | t <sub>CK(avg)</sub>       | -   |   | ps                   |
| Clock Period   | t <sub>CK(abs)</sub>       | t <sub>CK(avg) min</sub> + t <sub>JIT(per)min</sub> | t <sub>CK(avg) max</sub> + t <sub>JIT(per)max</sub> | ps                   |
| Average high pulse width                               | t <sub>CH(avg)</sub>       | 0.47  | 0.53  | t <sub>CK(avg)</sub> |
| Average low pulse width                                | t <sub>CL(avg)</sub>       | 0.47  | 0.53  | t <sub>CK(avg)</sub> |
| Clock Period Jitter                                    | t <sub>JIT(per)</sub>      | -80   | 80  | ps                   |
| Clock Period Jitter during DLL locking period          | t <sub>JIT(per, lck)</sub> | -80   | 80  | ps                   |
| Cycle to Cycle Period Jitter                           | t <sub>JIT(cc)</sub>       | 160   | -   | ps                   |
| Cycle to Cycle Period Jitter during DLL locking period | t <sub>JIT(cc, lck)</sub>  | 140   | -   | ps                   |
| Cumulative error across 2 cycles                       | t <sub>ERR(2per)</sub>     | - 118   | 118   | ps                   |
| Cumulative error across 3 cycles                       | t <sub>ERR(3per)</sub>     | - 140   | 140   | ps                   |
| Cumulative error across 4 cycles                       | t <sub>ERR(4per)</sub>     | - 155   | 155   | ps                   |
| Cumulative error across 5 cycles                       | t <sub>ERR(5per)</sub>     | - 168   | 168   | ps                   |
| Cumulative error across 6 cycles                       | t <sub>ERR(6per)</sub>     | - 177   | 177   | ps                   |
| Cumulative error across 7 cycles                       | t <sub>ERR(7per)</sub>     | - 186   | 186   | ps                   |
| Cumulative error across 8 cycles                       | t <sub>ERR(8per)</sub>     | - 193   | 193   | ps                   |
| Cumulative error across 9 cycles                       | t <sub>ERR(9per)</sub>     | - 200   | 200   | ps                   |
| Cumulative error across 10 cycles                      | t <sub>ERR(10per)</sub>    | - 205   | 205   | ps                   |

**11.2 AC Timing Parameters & Specifications (con't)**

| Parameter   | Symbol      | DDR3-1333  |      | Units    |
|---|-------------|--|------|----------|
|   |             | min  | max  |          |
| Cumulative error across 11 cycles                                       | tERR(11per) | - 210  | 210  | ps       |
| Cumulative error across 12 cycles                                       | tERR(12per) | - 215  | 215  | ps       |
| Cumulative error across n = 13, 14 ... 49, 50 cycles                    | tERR(nper)  | tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min<br>tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max |      | ps       |
| Absolute clock HIGH pulse width   | tCH(abs)    | 0.43   | -    | tCK(avg) |
| Absolute clock Low pulse width  | tCL(abs)    | 0.43   | -    | tCK(avg) |
| <b>Data Timing</b>  |             |  |      |          |
| DQS, /DQS to DQ skew, per group, per access                             | tDQSQ       | -  | 125  | ps       |
| DQ output hold time from DQS, /DQS                                      | tQH         | 0.38   | -    | tCK(avg) |
| DQ low-impedance time from CK, /CK                                      | tLZ(DQ)     | -500   | 250  | ps       |
| DQ high-impedance time from CK, /CK                                     | tHZ(DQ)     | -  | 250  | ps       |
| Data setup time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels        | tDS(base)   | TBD  | -    | ps       |
| Data hold time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels         | tDH(base)   | TBD  | -    | ps       |
| DQ and DM Input pulse width for each input                              | tDIPW       | 400  | -    | ps       |
| <b>Data Strobe Timing</b>   |             |  |      |          |
| DQS, /DQS READ Preamble   | tRPRE       | 0.9  | -    | tCK      |
| DQS, /DQS differential READ Postamble                                   | tRPST       | 0.3  | -    | tCK      |
| DQS, /DQS output high time  | tQSH        | 0.4  | -    | tCK(avg) |
| DQS, /DQS output low time   | tQSL        | 0.4  | -    | tCK(avg) |
| DQS, /DQS WRITE Preamble  | tWPRE       | 0.9  | -    | tCK      |
| DQS, /DQS WRITE Postamble   | tWPST       | 0.3  | -    | tCK      |
| DQS, /DQS rising edge output access time from rising CK, /CK            | tDQSCK      | -255   | 255  | ps       |
| DQS, /DQS low-impedance time (Referenced from RL-1)                     | tLZ(DQS)    | -500   | 250  | ps       |
| DQS, /DQS high-impedance time (Referenced from RL+BL/2)                 | tHZ(DQS)    | 250  | -    | ps       |
| DQS, DQS differential input low pulse width                             | tDQSL       | 0.45   | 0.55 | tCK      |
| DQS, DQS differential input high pulse width                            | tDQSH       | 0.45   | 0.55 | tCK      |
| DQS, DQS rising edge to CK, CK rising edge                              | tDQSS       | -0.25  | 0.25 | tCK(avg) |
| DQS, DQS falling edge setup time to CK, CK rising edge                  | tDSS        | 0.2  | -    | tCK(avg) |
| DQS, DQS falling edge hold time to CK, CK rising edge                   | tDSH        | 0.2  | -    | tCK(avg) |
| DLL locking time  | tDLLK       | 512  | -    | nCK      |
| internal READ Command to PRECHARGE Command delay                        | tRTP        | max<br>(4tCK, 7.5ns)   | -    |          |
| Delay from start of internal write transaction to internal read command | tWTR        | max<br>(4tCK, 7.5ns)   | -    |          |
| WRITE recovery time   | tWR         | 15   | -    | ns       |
| Mode Register Set command cycle time                                    | tMRD        | 4  | -    | nCK      |
| Mode Register Set command update delay                                  | tMOD        | max<br>(12tCK, 15ns)   | -    |          |
| CAS# to CAS# command delay  | tCCD        | 4  | -    | nCK      |
| Auto precharge write recovery + precharge time                          | tDAL(min)   | WR + roundup (tRP / tCK(AVG))  |      | nCK      |

**11.3 AC Timing Parameters & Specifications (con't)**

| Parameter  | Symbol             | DDR3-1333                  |         | Units |
|--|--------------------|----------------------------|---------|-------|
|  |                    | min                        | max     |       |
| Multi-Purpose Register Recovery Time   | tMPRR              | 1                          | -       | nCK   |
| ACTIVE to PRECHARGE command period   | tRAS               | 36                         | 70,000  | ns    |
| ACTIVE to ACTIVE command period for 1KB page size  | tRRD               | max<br>(4tCK,6ns)          | -       |       |
| ACTIVE to ACTIVE command period for 2KB page size  | tRRD               | max<br>(4tCK,7.5ns)        | -       |       |
| Four activate window for 1KB page size   | tFAW               | 30                         | -       | ns    |
| Four activate window for 2KB page size   | tFAW               | 45                         | -       | ns    |
| Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels  | tIS(base)          | 65                         | -       | ps    |
| Command and Address hold time from CK, CK referenced to Vih(ac) / Vil(ac) levels   | tIH(base)          | 140                        | -       | ps    |
| Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels  | tIS(base)<br>AC150 | 65+125                     | -       | ps    |
| Control & Address Input pulse width for each input   | tIPW               | 620                        | -       | ps    |
| <b>Calibration Timing</b>  |                    |                            |         |       |
| Power-up and RESET calibration time  | tZQinitI           | 512                        | -       | tCK   |
| Normal operation Full calibration time   | tZQoper            | 256                        | -       | tCK   |
| Normal operation short calibration time  | tZQCS              | 64                         | -       | tCK   |
| <b>Reset Timing</b>  |                    |                            |         |       |
| Exit Reset from CKE HIGH to a valid command  | tXPR               | max(5tCK, tRFC+<br>10ns)   | -       |       |
| <b>Self Refresh Timing</b>   |                    |                            |         |       |
| Exit Self Refresh to commands not requiring a locked DLL   | tXS                | max(5tCK,tRFC+<br>10ns)    | -       |       |
| Exit Self Refresh to commands requiring a locked DLL   | tXSDLL             | tDLL(min)                  | -       | nCK   |
| Minimum CKE low width for Self refresh entry to exit timing  | tCKESR             | tCKE(min) +<br>1tCK        | -       |       |
| Valid Clock Requirement after Self Refresh Entry (SRE)   | tCKSRE             | max(5tCK,<br>10ns)         | -       |       |
| Valid Clock Requirement before Self Refresh Exit (SRX)   | tCKSRX             | max(5tCK,<br>10ns)         | -       |       |
| <b>Power Down Timing</b>   |                    |                            |         |       |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP                | max<br>(3tCK,6ns)          | -       |       |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL   | tXPDLL             | max(10tCK, 24ns)           | -       |       |
| CKE minimum pulse width  | tCKE               | max(3tCK, 5.625ns)         | -       |       |
| Command pass disable delay   | tCPDED             | 1                          | -       | nCK   |
| Power Down Entry to Exit Timing  | tPD                | tCKE(min)                  | 9*tREFI | tCK   |
| Timing of ACT command to Power Down entry  | tACTPDEN           | 1                          | -       | nCK   |
| Timing of PRE command to Power Down entry  | tPRPDEN            | 1                          | -       | nCK   |
| Timing of RD/RDA command to Power Down entry   | tRDPDEN            | RL + 4 + 1                 | -       |       |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)  | tWRPDEN            | WL + 4 +(tWR/tCK)          | -       | nCK   |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)   | tWRAPDEN           | WL + 4 +WR+1               | -       | nCK   |
| Timing of WR command to Power Down entry (BL4MRS)  | tWRPDEN            | WL + 2 +(tWR/<br>tCK(avg)) | -       | nCK   |



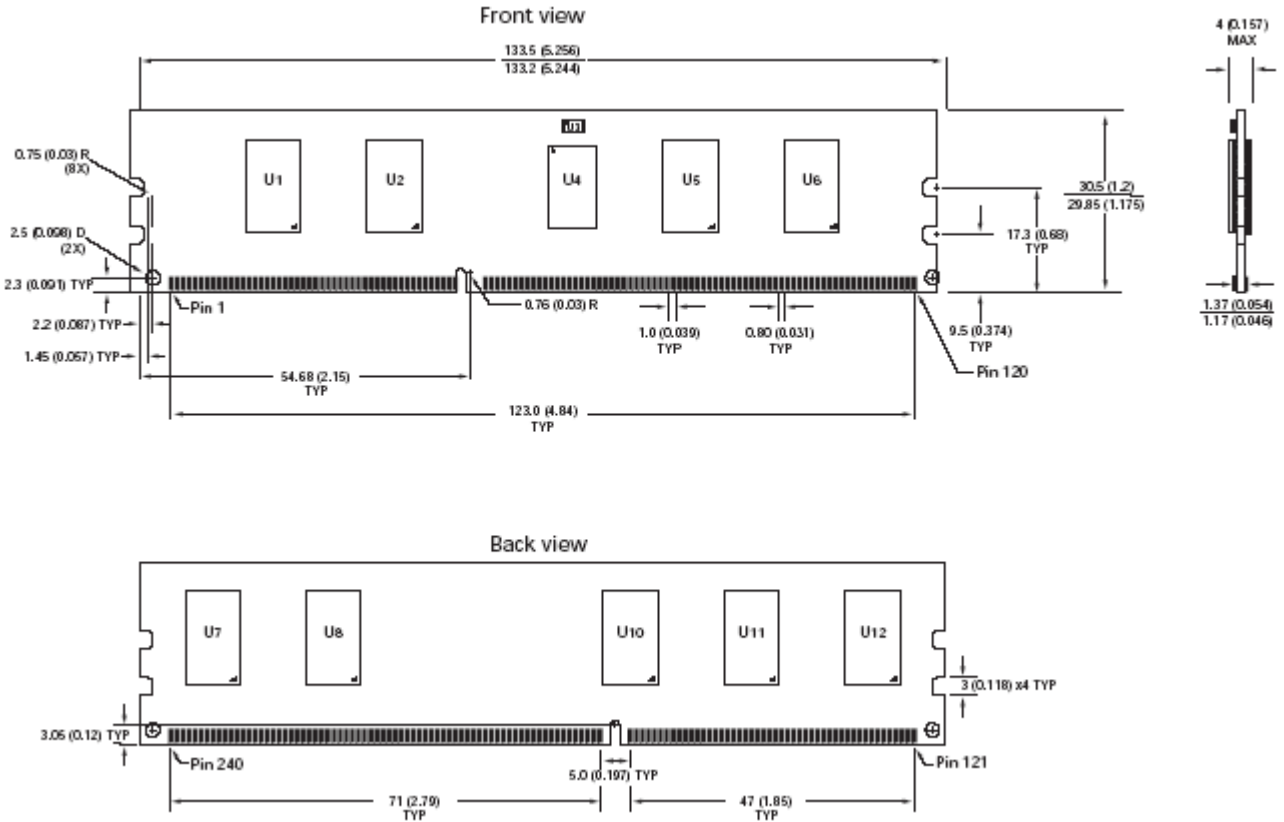
**11.4 AC Timing Parameters & Specifications (con't)**

| Parameter  | Symbol   | DDR3-1333    |     | Units    |
|--|----------|--------------|-----|----------|
|  |          | min          | max |          |
| Timing of WRA command to Power Down entry(BL4MRS)                    | tWRAPDEN | WL +2 +WR +1 | -   | nCK      |
| Timing of REF command to Power Down entry                            | tREFPDEN | 1            | -   |          |
| Timing of MRS command to Power Down entry                            | tMRSPDEN | tMOD(min)    | -   |          |
| <b>ODT Timing</b>  |          |              |     |          |
| ODT high time without write command or with write command and BC4    | ODTH4    | 4            | -   | nCK      |
| ODT high time with Write command and BL8                             | ODTH8    | 6            | -   | nCK      |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen)          | tAONPD   | 1            | 9   | ns       |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen)         | tAOFPD   | 1            | 9   | ns       |
| ODT turn-on  | tAON     | -250         | 250 | ps       |
| RTT_NOM and RTT_WR turn-off time from ODTL off reference             | tAOF     | 0.3          | 0.7 | tCK(avg) |
| RTT dynamic change skew  | tADC     | 0.3          | 0.7 | tCK(avg) |
| <b>Write Leveling Timing</b>   |          |              |     |          |
| First DQS pulse rising edge after tDQSS margining mode is programmed | tWLMRD   | 40           | -   | tCK      |
| DQS/DQS delay after tDQS margining mode is programmed                | tWLDQSEN | 25           | -   | tCK      |
| Setup time for tDQSS latch   | tWLS     | 195          | -   | ps       |
| Hold time of tDQSS latch   | tWLH     | 195          | -   | ps       |
| Write leveling output delay  | tWLO     | 0            | 9   | ns       |
| Write leveling output error  | tWLOE    | 0            | 2   | ns       |

## 240-Pin DDR3- Reg/ECC-DIMM

## DDR3 SDRAM

### 12.0 Physical Dimensions: (128Mx8 Based) 128Mx72 (1 Rank)



Tolerances:  $\pm 0.005(.13)$  unless otherwise specified